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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,394	01/16/2002	Michael Fliesler	F0466	6188

7590 07/08/2003

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,394	FLIESLER ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *9-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-2, 4-8 is/are rejected.

7)☒ Claim(s) 3 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *16 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other.

DETAILED ACTION

1. The amendment filed on 04/24/03 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1,2,4 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over THE ADMITTED PRIOR ART in view of TAHARA et al. and KUBO et al.

The admitted prior art discloses a system for protecting an integrated circuit from electrostatic discharge with a core region (DIE CORE); a pad (PAD) electrically coupled to the core region (DIE CORE) through an input device (THE INVERTER CONSISTING OF PMOS AND NMOS TRANSISTORS 16 AND 18), the input device having at least one CMOS device with a gate oxide layer; and at least one protection diode 12, 14 operable to provide a discharge path for electrostatic discharge due to a high voltage being applied to the pad, the at least one diode comprising a first diode 12 and a second diode 14 forming an input protection circuit adapted to protect the input device, and the input device being a CMOS inverter formed from the aforesaid PMOS an NMOS transis-

tors. Note figure 1 of the instant application. The admitted prior art does not disclose that the at least one protection diode has a reverse breakdown voltage less than the breakdown voltage of the gate oxide layer, nor that the reverse breakdown voltage of the at least one diode is greater than the supply voltage Vcc.

However, Tahara et al. discloses a system for protecting an integrated circuit from electrostatic discharge comprising a protected circuit having a transistor with gate oxide 12, and an input protection circuit comprising at least one protection diode D with a reverse breakdown voltage which is lower than the insulation breakdown voltage of the gate oxide 12 and higher than the supply voltage. Note figure 27 and column 1 lines 43-47 of Tahara et al.. Therefore, it would have been obvious to a person having skill in the art to provide the at least one protection diode of the admitted prior art's system for protecting an integrated circuit from electrostatic discharge with the reverse breakdown voltage in the range less than the breakdown voltage of the gate oxide layer and greater than the supply voltage Vcc such as taught by Tahara et al. One would have been motivated to make this substitution by, for example, the teaching of Kubo et al., which states that "[when] a surge voltage, which is caused, for example, by an electric charge accumulated on the human body of an operator handling the device or by an AC supply voltage induced through a soldering iron during the mounting of the device on a printed board, makes the electric potential of the gate electrode 4 as high as the breakdown voltage of the gate insulator 8 before the electric potential of the diode 6 reaches its reverse breakdown voltage ... [t]he gate insulator 8, therefore, breaks down, the protecting

function of the diode [in such case] being useless." Note column 2 lines 5-30 of Kubo et al.

B. Claims 5,6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over THE ADMITTED PRIOR ART in view of TAHARA et al. and KUBO et al. as applied to claim 1 above, and further in view of ITO ET AL. (5,416,351).

The admitted prior art in view of Tahara et al. and Kubo et al. suggests a system for protecting an integrated circuit from electrostatic discharge having all the limitations of claims 5,6, and 8 except that the at least one diode comprises a power supply clamp diode, the at least one diode comprising a heavily doped N++ region and a heavily doped P++ region, and that the core region comprises a flash memory device.

However, Ito et al. discloses a system for protecting an integrated circuit from electrostatic discharge with at least one diode comprising a power supply clamp diode, the at least one diode comprising a heavily doped N region 202 and a heavily doped P region (PBASE), and a core region comprising a flash memory device. Note figure 27A and column 22 line 65 of Ito et al. Therefore, it would have been obvious to a person having skill in the art to augment the system for protecting an integrated circuit from electrostatic discharge suggested by the admitted prior art, Tahara et al., and Kubo et al., with the at least one diode comprising a power supply clamp diode, the at least one diode comprising a heavily doped N region and a heavily doped P region and core region comprising a flash memory device such as taught by Ito et al. in order to provide a compact ESD protection device (the clamp diode utilizing heavily doped "Zener" diodes

being capable of shunting more current in a smaller space than an ordinary diode, as Ito et al. point out) to thus provide better ESD protection.

Allowable Subject Matter

3. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments with respect to the § 103 rejections of claims 1,2,4, and 7 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments and clarifying remarks with respect to the § 112 rejection of claim 3 appear well founded. Given the meaning of this claim as applicant explains it, this claim is considered allowable.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.Any inquiry concerning this communication or earlier communications from the examiner should be directed to

Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
06/2003

Minhloan Tran
Primary Examiner
Art Unit 2826